**Step 1: Determine architecture**

Load regulation

, where and

To save power and avoid creating too much poles, I chose a triple cascode telescopic amplifier as the error amplifier over folded cascode and multiple stage.

**Step2: Choose parameters**

make it 43 to make sure that the gain will be good enough.

Since we are triple cascoding, choose =0.2V, Δ=0.1V so that there is enough space for all transistors to be biased in saturation.

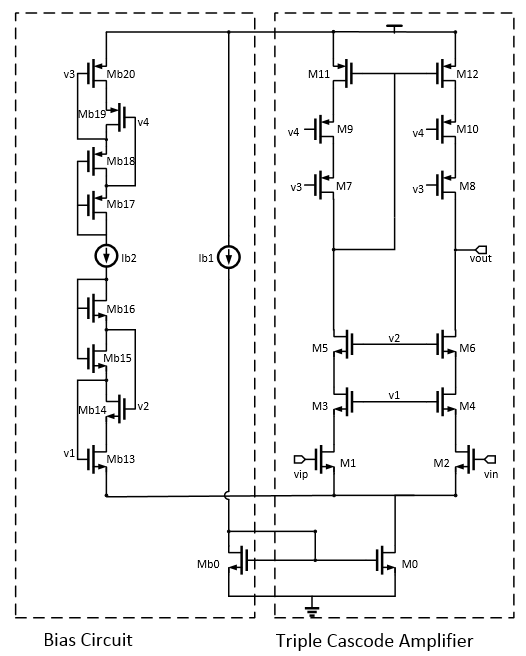
Plug , =0.2V, Δ=0.1V in to the Matlab lookup table, we can get the minimum length .

, and is the for the pass transistor.

PSR@1MHz =-20dB and worst case PSR =0dB, which will be at , so is 10 times bigger than 1MHz, which gives us 10MHz.

, =0.152 m=. Thus, , and then I got the width of the NMOS to be 2.9

Step3: design circuits, simulate and modify



In order to save power, I used minimum size for the bias circuit. For Mb15, the size is x to make the effective size of Mb16 in series with Mb15 to be 4x. This is also true for Mb17 and Mb18 for PMOS. After simulation, I found v1 too high and v3 too low, which in turn compressed for M1 and M2 and for M11 and M12, so I made Mb13 and Mb20 slightly smaller. Finally, I found the gain not enough at the output, so I made the length for all transistors to be slightly larger, 360nM.

|  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- |
|  | Size | Bias Current |  |  | region |
| M0 |  |  |  | 88.37mV | 2 |
| M1 |  |  |  | 78.64m |
| M2 | 78.65m |
| M3 |  | 79.95m |
| M4 | 80.04m |
| M5 |  | 77.46m |
| M6 | 78.18m |
| M7 |  |  | -105.5m |
| M8 |  | -103.2m |
| M9 |  | -103.2m |
| M10 | -103.1m |
| M11 |  | -98.68m |
| M12 |  | -98.68m |
| Mb0 |  |  |  | 89.32m |
| Mb13 |  |  |  | 179.6m | 1 |
| Mb14 |  |  | 128.4m | 2 |
| Mb15 |  |  | 235.1m | 1 |
| Mb16 |  |  | 133.4m | 2 |
| Mb17 |  |  | -197.5m | 2 |
| Mb18 |  |  | -377.4m | 1 |
| Mb19 |  |  | -185.5m | 2 |
| Mb20 |  |  | -305.7m | 1 |