**Step 1: Determine architecture**

Load regulation

, where and

To save power and avoid creating too much poles, I chose a triple cascode telescopic amplifier as the error amplifier over folded cascode and multiple stage.

**Step2: Choose parameters**

make it 43 to make sure that the gain will be good enough.

Since we are triple cascoding, choose =0.2V, Δ=0.1V so that there is enough space for all transistors to be biased in saturation.

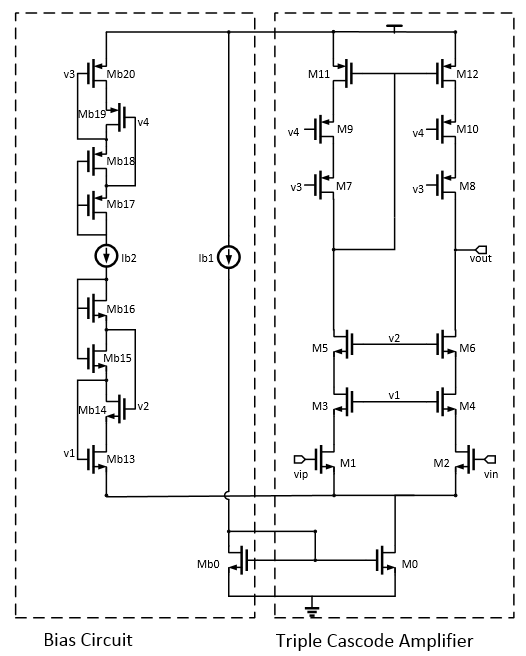
Plug , =0.2V, Δ=0.1V in to the Matlab lookup table, we can get the minimum length .

, and is the for the pass transistor.

PSR@1MHz =-20dB and worst case PSR =0dB, which will be at , so is 10 times bigger than 1MHz, which gives us 10MHz.

, =0.152 m=. Thus, , and then I got the width of the NMOS to be 2.9

Step3: design circuits, simulate and modify



In order to save power, I used minimum size for the bias circuit. For Mb15, the size is x to make the effective size of Mb16 in series with Mb15 to be 4x. This is also true for Mb17 and Mb18 for PMOS. After simulation, I found v1 too high and v3 too low, which in turn compressed for M1 and M2 and for M11 and M12, so I made Mb13 and Mb20 slightly smaller. Finally, I found the gain not enough at the output, so I made the length for all transistors to be slightly larger, 360nM.